REMARKS

This Response responds to the Office Action dated September 22, 2006 in which the Examiner rejected claims 1-13 under 35 U.S.C. §103.

Claims 1 and 13 claim an image forming apparatus and claim 8 claims an image processing method. The image apparatus and method includes determining whether a target pixel belongs to a dot area based upon extracted dot characteristic points and setting N-level conversion parameters based on results of the determination of the target area belonging to the dot area.

Through the structure and method of the claimed invention determining if a target pixel belongs to a dot area based on extracted characteristic points and setting N-level conversion parameters based on the results of the determination as claimed in claims 1, 8 and 13, the claimed invention provides an image processing apparatus and method which can prevent a moiré phenomena from occurring when the image data in a dot area is converted into an N-level image data. The prior art does not show, teach or suggest the invention as claimed in claims 1, 8 and 13.

Claims 1-13 were rejected under 35 U.S.C. §103 as being unpatentable over *Kojima* (U.S. Patent 5,454,052).

Applicant respectfully traverses the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicant respectfully requests the Examiner withdraws the rejection to the claims and allows the claims to issue.

Kojima appears to disclose in Figure 1 four line memories 11-14 and a feature extraction circuit 8 for extracting the features proximal to a target pixel of N-value (binary) image data. In particular, based upon five windows, the feature extraction

circuit 8 extracts a horizontal edge feature and a vertical edge feature (column 5, lines 21-44). Thus, nothing in *Kojima* shows, teaches or suggests determining whether a target pixel belongs to a dot area based upon the results of extracting dot characteristic points as claimed in claims 1, 8 and 13. Rather, the feature extraction circuit 8 in *Kojima* is for extracting edge features. The feature extraction circuit 8 of *Kojima* does not determine whether the pixel belongs to a dot area based upon extracted dot characteristic points.

Furthermore, *Kojima* merely discloses an error suppressor 110 which enhances edge components in the input image data by means of edge enhancement circuit 112. The edge area of the input image data is detected by the edge detection 111, which output signal EGL. The mixing circuit 113 changes the mixing ratio of the input image data input B and the data input A output from the edge enhancement circuit 112 based on the input EGL from the edge detection circuit 111 and outputs the K-valued image data X. The mixing ratio of the inputs A and B is set by the output from the image quality controller 62 based upon outputs from keyboard 63 (column 10, line 59 through column 11, line 10). Thus *Kojima* merely discloses an error suppressor 110 which outputs enhanced edge components as K-valued image data. Thus nothing in *Kojima* shows, teaches or suggests setting conversion parameters used in an N-level conversion unit based on the results of a determination whether a target pixel belongs to a dot area as claimed in claims 1, 8 and 13. Rather, the error suppressor 110 of *Kojima* merely enhances edge components based upon outputs from a keyboard 63.

Finally, Applicant respectfully traverses the Examiner's characterization of *Kojima*. Applicant notes that Figure 1a of *Kojima* shows line memories 11-14,

feature extraction circuit 8, evaluation circuits 1, 3, 5, normalization circuits 2, 4, 6 and mixer 7. Additionally, Figure 6 shows similar features with memory 65, feature extraction units 19a, 19b, evaluation circuits 16a, 16b, normalization circuits 17a, 17b and mixer 68. Additionally, Figure 6 of *Kojima* shows an N-value conversion circuit 64 which outputs to memory 65. Therefore, the error suppressor 110 in Figure 6 of *Kojima* occurs prior to the image data being input into memory 65. Thus, the characterization of *Kojima* by the Examiner is inaccurate since the Examiner states that the feature extraction unit 8, 19a, 19b is analogous to the dot area identifying device claimed in claims 1, 8 and 13. In other words, the parameter setting unit as claimed in claims 1, 8 and 13 sets parameters based upon the output from the dot area identifying device. However, the feature extraction unit 8, identified by the Examiner as the dot area identifying device, does **not** output to the N-value converting unit 64. Furthermore, the error suppressor 110 in Figure 6 of *Kojima,* which does output a result to the N-value conversion circuit 64, does not determine whether a target pixel belongs to a dot area based upon an extraction of dot characteristic points. Rather, error suppressor 110 of *Kojima* merely has enhanced edge detection.

Since nothing in *Kojima* shows, teaches or suggests a) determining whether target pixels belongs to a dot area based upon extracted dot characteristic points and b) setting N-level conversion parameters based upon results of the determination for the target pixel belonging to the dot area as claimed in claims 1, 8 and 13, Applicant respectfully requests the Examiner withdraws the rejection to claims 1, 8 and 13 under 35 U.S.C. §103.

Claims 2-7 and 9-12 depend from claims 1 and 8 and recite additional features. Applicant respectfully submits that claims 2-7 and 9-12 would not have been obvious or anticipated by *Kojima* within the meaning of 35 U.S.C. §103 at least for the reasons as set forth above with respect to claims 1 and 8. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 2-7 and 9-12 under 35 U.S.C. §103.

The prior art of record, which is not relied upon, is acknowledged. The reference taken singularly or in combination does not anticipate or make obvious the claimed invention.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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